

# ADVANCED MICROELECTRONICS TECHNOLOGIES FOR FUTURE SMALL SATELLITE SYSTEMS

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## ABSTRACT

Future **small satellite systems** for both Earth observation as well as deep-space exploration are greatly enabled by the technological advances in deep sub-micron **microelectronics** technologies. Whereas these technological advances are being fueled by the commercial (non-space) industries, more recently there has been an exciting new synergism evolving between the two otherwise disjointed markets. In other words, both the commercial and space industries are enabled by advances in low-power, highly integrated, miniaturized (low-volume), lightweight, and reliable real-time embedded systems. Recent announcements by commercial semiconductor manufacturers to introduce **Silicon On Insulator (SOI)** technology into their commercial product lines is driven by the need for high-performance low-power integrated devices. Moreover, SOI has been the technology of choice for many space semiconductor manufacturers where radiation requirements are critical. This technology has inherent radiation latch-up immunity built into the process, which makes it very attractive to space applications. In this paper, we describe the advanced microelectronics and avionics technologies under development by NASA's **Deep Space Systems Technology Program** (also known as **X2000**). These technologies are of significant benefit to both the commercial satellite as well as the deep-space and Earth orbiting science missions. Such a synergistic technology roadmap may truly enable quick turn-around, low-cost, and highly capable small satellite systems for both Earth observation as well as deep-space missions.

## 1. INTRODUCTION

NASA's drive towards more frequent smaller missions (*faster-better-cheaper*) for both space science as well as Earth science is revolutionizing many aspects of space exploration. One benefit of having more frequent missions is the opportunity for more frequent technology insertion. That is, if a mission takes 5 – 10 years to build and launch, the technology used may be commercially obsolete by the time of launch. On the other hand, having multiple launches a year enables new technology insertion as it becomes mature. This is especially true for the fast developing field of commercial microelectronics technologies.

The United States National Technology Roadmap for Semiconductors [1] still projects the continued reduction of the minimum semiconductor device features size ( $\lambda$ ) by a factor of  $s = \sqrt{2}/2$  every three years up to 2012. This market and technology-

driven phenomenon, referred to as Moore's Law, was first observed by Gordon Moore, one of the co-founders of Intel Corporation, in the early 60s. Sustained reduction of the minimum feature size enables higher levels of functional integration on a single chip (integrated circuit). Moreover, higher volumes of production, better manufacturing capabilities and improved reliability leads to lower cost. Therefore, the net result: more for less, has been the main fuel behind the microelectronics technological revolution of the 20<sup>th</sup> century.

Because of the uniquely harsh requirements of space applications (radiation, thermal, vibration, reliability, etc.), it was generally considered that commercial products based on commercial semiconductor technology are not readily applicable to space. Whereas this is generally correct, recent trends both in the commercial consumer sector, as well as in the space science and technology sector, are moving the two (otherwise disjoint) underlying technologies closer together. For example, portable and mobile computing platforms in the consumer industries are stimulating the development of low-power, energy-efficient, reliable, high-performance, embedded (real-time), highly miniaturized, and light-weight, modular and upgradable computer systems. All of these attributes have become essential requirements in the development of low-cost space science and commercial satellite systems.

In this paper, we initially describe a new program at NASA designed to develop new mission-enabling spacecraft systems every three years. This program called Deep Space Systems Technology Program, and commonly referred to as X2000, is managed at NASA's Jet Propulsion Laboratory. A major emphasis of X2000 is the development and insertion of new microelectronics and micro-avionics technologies into future missions. This work is performed by the newly formed Center for Integrated Space Microsystems (CISM) [2] described in Section 3. In Section 4, we describe the X2000/CISM micro-avionics technology roadmap through three generations of spacecraft systems. Finally, we offer our concluding remarks in Section 5.

## **2. NASA'S DEEP SPACE SYSTEMS PROGRAM (X2000)**

Starting in fiscal year 1998, NASA initiated a new focused deep-space systems technology program as part of the NASA Office of Space Science Directorate. This program, also referred to as X2000, has as its goal to develop new generations of spacecraft systems, on three year intervals, that will enable future deep-space science missions [3]. Functionally, the program has three major elements: 1) an element focused on delivering new generations of flight-ready spacecraft systems called: X2000 1st, 2nd, 3rd , ... Delivery Projects; 2) a Center for delivering Integrated Space Micro-systems (CISM) for the flight-systems as well as research micro-avionics technologies for future missions; and 3) a program focused on delivering new Advances in Radio-isotopic Power Sources (ARPS) [4]. The X2000 1st Delivery Project is well under way [5], whereas the 2nd Delivery Project is expected to be initiated later this year. One of the goals of the X2000 Program as a whole, is to make a major technology push towards highly integrated Systems On A Chip. This technology is part of the newly formed center CISM, described in the following section.

### **3. CENTER FOR INTEGRATED SPACE MICROSYSTEMS (CISM)**

The newly formed center for integrated space microsystems (CISM) is an element of the X2000 Program, as well as a Center of Excellence at the Jet Propulsion Laboratory [6]. CISM currently supports the following three major technology thrust initiatives:

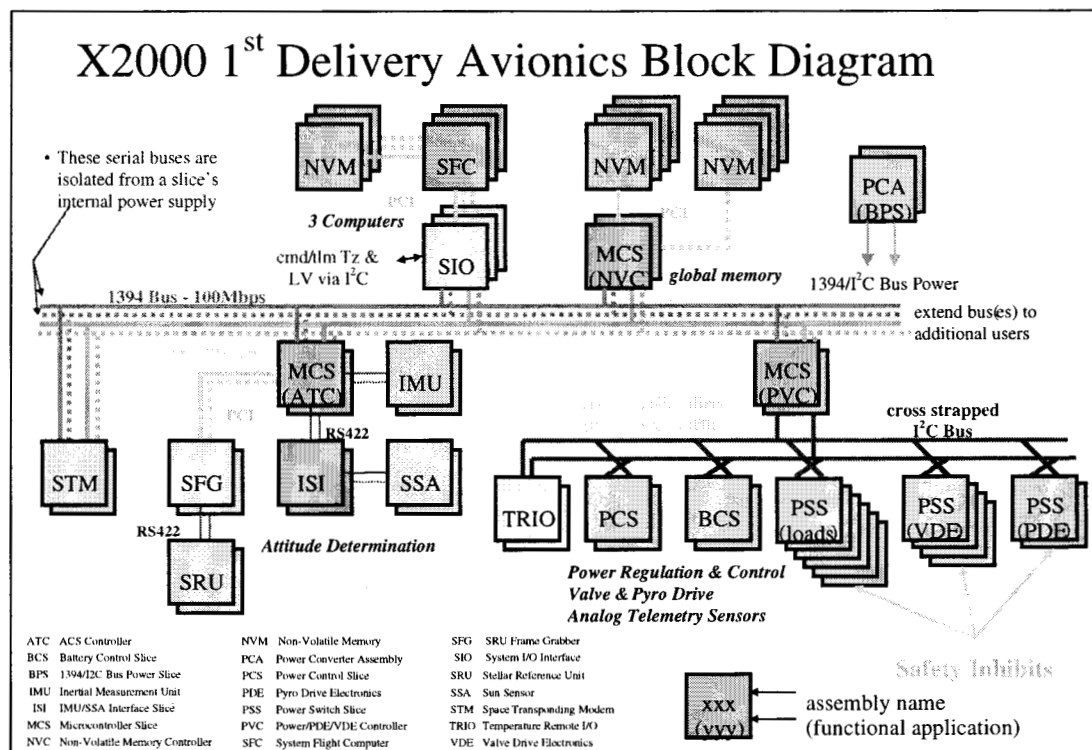
1. Near-Term avionics deliverables to flight projects.
2. Systems On A Chip (mid-term research) technologies for future flight projects.
3. Revolutionary Computing Technologies (long-term, basic research) with potential breakthroughs in 10 years or beyond.

#### **3.1 Near-Term Research and Development**

The avionics architecture, shown in Figure 1 below, for the 1st Delivery Project has already been selected, with the architectural baseline established at the Avionics Preliminary Design Review (PDR) held in August 1998. Even though revisions to the proposed baseline architecture are still being considered, the essential components are expected to remain the same. The X200 avionics shown in Figure 1 implements the main spacecraft control, communications, and monitoring functions. That is, it implements the traditional spacecraft functions of a Command Data Handling Subsystem (CDH), the Power Control and Distribution Subsystem, Attitude Control, Signal Processing, etc. This avionics architecture is both general enough and scaleable to accommodate flight projects of different requirements, including: Europa Orbiter, New Millennium Program Deep Space 4, Mars Sample Return, Pluto/Kuiper Express, Solar Probe, and others. The 1st Delivery Avionics architecture is characterized by the following attributes:

- A Distributed, symmetric architecture, with computing nodes and device nodes sharing a common bus architecture. The number of nodes and devices on the bus are scaleable, [7].
- Use of exclusively commercial off the shelf (COTS) interfaces and intellectual properties (IP) for their implementation on a radiation-hardened semiconductor foundry. The COTS interfaces include: 1394, IIC, JTAG, and PCI local bus. The buses are redundant in the baseline.
- Next generation System Flight Computer (SFC) with an order of magnitude improvement over existing state of the art computer performance. A baseline target performance of > 100 MIPS (goal 200 MIPS) is under development. The advanced 32-bit computer will be built in a standard Compact PCI 3U format. This will facilitate and reduce the cost of early development, system integration and test, as well as the avionics system recurring cost.
- Next generation integrated packaging technology using Compact PCI (CPCI) backplane technology with enhancements for conductive cooling. This packaging is compliant with the standard CPCI backplane.
- Next generation micro-controller technology for embedded intelligent devices.
- Advanced integrated non-volatile memory systems.
- Highly integrated Power Activation and Switching Modules using solid state devices and High Density Interconnect technologies.
- Advanced Silicon On Insulator (SOI) semiconductor technology for low-power, high-performance integrated circuit design.

- Advanced digital ASIC technology for over 1.0 – 1.5 M gates integrated on a single chip.
- Advanced mixed/signal ASIC technology for integrated power electronics.



**Figure 1. X2000 1<sup>st</sup> Delivery Avionics Architecture Block Diagram**

### 3.2 Systems On A Chip: Mid-Term R&D

The Systems On A Chip program targets future X2000 deliverables, starting with the 2<sup>nd</sup> in 2003 [8], and the 3<sup>rd</sup> in 2006. The elements of this research program include:

- RF Front-End miniaturization using micro-machining and thin film technologies.
- Micro Inertial Reference Systems (IRS) using MEMS technology.
- Integrated Multifunctional Imaging using Active Pixel Sensor (APS) technology.
- Integrated Passive Components using thin film micro-magnetics.
- Highly integrated power electronics using mixed signal ASIC technologies.
- Integrated sensor technologies for environmental, chemical, biological sensing and monitoring.
- Low Power devices, circuits, architectures, and components.
- Advanced design, integration and test technologies for systems on a chip.
- Design for high-yield and high-reliability; co-design and co-verification methodologies.
- And other integrated microsystems technologies.
- Design reuse for Systems On a Chip, using commercial IPs, soft cores, etc.

### 3.3 Revolutionary Computing Technologies: Basic Research

The Revolutionary Computing Technologies program is addressing basic research problems for future long-term computing needs in space applications. Several 'Grand Challenge' problems have been identified in this area:

- Sensing of Bio-Molecular Signatures for the identification of life.
- Ultra Reliable, Survivable microelectronics for long-term inter-stellar exploration, with survivability goals of 40 – 100 years in outer space.
- Evolvable hardware circuits and microsystems.
- Quantum Functional Devices: Quantum Dots for low-power highly integrated systems.
- Quantum Computation and Communications.
- Optical Computing, Storage, and Communications.
- Biological Computing: DNA Computing.
- Bio-Mimetics, Bio-Informatics, etc.

In Table 1 below, we present an integrated technology roadmap for microelectronics systems throughout the 3 X2000 deliveries. Whereas the 1<sup>st</sup> Deliverable is somewhat firm, the 2<sup>nd</sup> and especially the 3<sup>rd</sup> Deliverable are currently being studied. Therefore, the inputs for these are only tentative, and are most certainly going to change.

#### **4. SYNERGISM WITH CONSUMER ELECTRONICS AND COMMERCIAL SPACE SECTORS**

More than ever before, it seems that the world of consumer microelectronics, commercial space systems, as well as deep-space and Earth orbiting science missions, have a consistent technology roadmap. In other words, all of these markets are greatly enabled by the development of technologies for higher levels of integration, miniaturization, reduction in mass, volume and power, higher reliability and on-board intelligence (autonomy) [9,10]. Moreover, from the semiconductor technology level, up to the avionics systems level, there seem to be very few points of departure.

Silicon On Insulator (SOI) technology has increasingly been the technology of choice for space applications due to its inherent immunity to single-event latch-up from high-energy particles. In fact, a low-power SOI experiment based on the 0.25 micron technology from MIT/LL is currently being validated on board the New Millennium DS1 mission [11]. The same technology has recently been announced as the choice for commercial semiconductor manufacturers due to its applicability to low-power high-performance devices.

Even at the component level, such as in the case of commercial DRAM technologies, newer generations of components such as 16 Mbit and 64 Mbit DRAMs, are no less prone to Single Event Upsets (SEU). This is because even at the commercial level, a floor has been reached due to the experience of SEUs caused by alpha particles on ground [12].

As demonstrated by the X2000 Program, more and more COTS technology is being used in space systems. The challenge for radiation intensive missions like Europa, is to use COTS IPs combined with radiation hard foundries, and minimum redesign of the interfaces, to achieve high levels of system reliability and radiation tolerance. Thus, at

the architectural level, the system is compatible with commercial designs. This will reduce system development time and cost, as well as reduce the total system recurring cost.

Technology	1 <sup>st</sup> Delivery (2000)	2 <sup>nd</sup> Delivery (2003)	3 <sup>rd</sup> Delivery (2006)
<b>Semiconductor</b>			
feature size	0.25um – 0.35um	0.18um – 0.25um	0.13um – 0.18um
process type	Bulk and SOI CMOS	SOI PD CMOS	SOI FD CMOS, SiGe
supply voltage	3.3 – 2.5 volts	2.5 - 1.5 volts	1.5 – 0.9 volts
LM (wafer size)	4 – 5 (6" – 8")	5 – 6 (8" – 10")	6 – 8 (10" – 12")
<b>RH Building Blocks</b>			
CPU	PPC 750/740, 603e, Pentium	32 bit CPU Core	64 bit – CPU Core
Micro-controller	32-bit high-performance	32-bit core	64-bit micro-controller core
SRAM	4 Mbit	16 Mbit	64 Mbit
ASIC: digital	1.0 – 1.5 M gates (0.35 um)	1.5 - 4.0 M gates (0.25 u)	4.0 - 8.0 M gates
ASIC: analog/mixed	0.8 um SOI mixed signal	0.35 SOI mixed signal	0.25 SOI mixed signal
DRAM: commercial	16, 64 Mbit	64 - 256 Mbit	256 Mb, 1 Gbit
Non-Volatile: Flash, etc.	64 Mbit	256 Mbit	1 Gbit
<b>COTS Interfaces</b>			
Local Bus	PCI 2.1 @ 33 Mhz, 64-b	High-Rel PCI	On-Chip PCI Core
Low Power Utility Bus	I2C	I2C	Distributed I2C
Eng. Bus	1394 100 Mbps	1394 400 Mbps	Multi-fiber optic links
High-Speed Bus	IEEE 1394	1 Gbps X-bar Switches	On-chip X-bar Switches
Test Bus	IEEE 1149.1 JTAG	IEEE 1149.1/5 JTAG	Macro Cell
<b>Advanced Packaging</b>			
Avionics Systems Packaging	Standard Compact PCI backplane (box)	Horizontally Mounted Cube (HMC) of Slices	Microelectronics embedded into multifunctional s/c
Board Level packaging	3U Compact PCI boards with conductive cooling	5"x5" slices with Z and Y axis interconnects	Distributed slices with flex interconnects in structure
Chip Scale Packaging	BGA, C4, Chip on Board, MCMs	BGA, C4, Chip on Board, MCMs	BGA, C4, Chip on Board, MCMs
3D Chip Stacking	4 - 48 IC per 3D memory stack	Memory and other IC in stack	Design for high-density 3D stack integration of ICs
<b>Design Automation</b>			
CAD	VHDL IC Models, Soft-Core IPs transfer to RH foundries	System-Level VHDL Models, RH IPs	System Level modeling and synthesis
Collaborative Eng.	Distributed Design	Virtual Skunk-works	Language to Layout
<b>Attitude Control</b>			
Star Tracker	Adv. Stellar Compass	Optical Processing	Integrated msystem
Sun Sensors/Gyros/Acc.	MEMS-based	MEMS-based	MEMS-based
<b>Fault Tolerance</b>			
FT Model	Distributed FT: 2-3 nodes	Distributed FT (n-nodes)	Distributed FT
SW FT Model	SW implemented FT	Design for Reliability	Design for Survivability
Techniques	Adaptive FT	Self Repair	Evolving – Immune based
Reliability Modeling	Partial Models	Integrated Tools Set	End-to-End Models
<b>Power Electronics</b>			
Power activation and switching modules (PASM)	16 solid state power switches	48 Switches	Switches on chip
Power management and distribution (PMAD)	High Efficiency DC/DC	High Efficiency DC/DC	PASM/PMAD on a Chip
Integration approach	High Density Interconnect (HDI)	High Density Interconnect (HDI)	Macro-cells integrated on a chip
<b>Telecom Processing</b>			
I/F to Avionics	RF interface via 1394 bus	Optical Com. I/F	On Chip Interface
<b>Enhancing Technologies</b>			
Neural Networks	Autonomy support	S/C Navigation	Learning Cells
DSPs	SHARC21060 – HDSP	Ultra SHARC	Standard Cell

**TABLE 1. Microsystems technology roadmap for the 1st, 2nd, and 3rd Avionics Deliveries.**

## 5. CONCLUSIONS

NASA's Deep Space Systems Technology Program, also known as X2000, is currently developing a series of advanced spacecraft systems for future deep-space science missions. An element of the X2000 Program is the newly formed Center for Integrated Space Microsystems (CISM). This center is responsible for the delivery of all spacecraft avionics to near-term missions launching in the 2003 time frame. Moreover, CISM is also placing major emphasis on future systems with technology development of Systems On A Chip, and Revolutionary Computing Technologies. The Avionics architecture described in this paper for the X2000 1<sup>st</sup> Delivery has numerous new technologies which are synergistic with the needs of the commercial satellite industries. Moreover, the technology roadmap for future space systems is compatible and synergistic in most ways, with recent developments in the commercial consumer electronics sectors. Examples include the use of advanced Silicon On Insulator (SOI) technology for integrated circuits, and components; commercial DRAM and Flash technology for volatile and non-volatile memory storage; Commercial Off The Shelf interfaces and IPs such as the 1394, IIC, 1149.1 JTAG, PCI, etc.; distributed, symmetric processing over a local-area network; and distributed fault-tolerance.

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